AD102 — Linear Circuits & Fabrication

You already know what a resistor does. This course is about what a resistor, a capacitor and an inductor are when they are built on silicon, and what each one costs in chip area.

The course is part of the **UofT ASIC Team** education materials, and it's published at **https://uoftasic.com/ad102/**. The labs run inside the **workbench**, which is the IIC-OSIC-TOOLS container you start from the `workspace` repo you set up in IC101.

Who this course is for

AD102 is the second course in the analog track, for 2nd–3rd year ECE students who have finished IC101 and AD101.

ECE110 teaches linear circuit analysis: node voltages, mesh currents, $V = IR$, RC time constants, impedance. AD102 doesn't teach any of that again, and it isn't a substitute for it. If you have taken ECE110 you are ahead, and if you haven't, AD101 already covered everything this course uses.

What ECE110 leaves out is where the components come from. In a lab kit, a resistor comes out of a drawer with its value printed on the side. On a chip there's no drawer to take it from: a resistor is a strip of doped polysilicon that you draw, and its value follows from the drawing, from how long and how wide the strip is and which layer it's on. Changing the shape is the only way you have to change the value. The idea that this whole course builds on is that **a component value is a geometry, and geometry costs area.**

On a breadboard, component values are free and independent of each other: a 10 kΩ costs the same as a 100 Ω, and you can have as many as you like. On silicon neither of those is true. A 1 pF capacitor is roughly a 22 µm × 22 µm plate: 484 µm² of silicon, which simulates at 982.5022 fF, a little short of 1 pF (Lab 02 gives you the formula behind that number, and sizes the plate exactly). The 4-bit ripple-carry adder that the digital track builds in DD103, twelve SKY130 standard cells, fits in 110.1056 µm² of the same process, so that one capacitor takes the area of 4.4 adders. The analog habits you'll pick up here all follow from that comparison: ratios instead of values, unit devices, and keeping inductors off the chip below a gigahertz.

At a glance

Track	Analog
Prerequisites	IC101 then AD101, in that order
Tools	ngspice and XSchem, both inside the workbench, plus SiliWiz (a browser layout tool that shows cross-sections) in a browser tab
PDK	SKY130 (`sky130A`), included in the image
Time	About 15.5 hours, self-paced
Math	Algebra, $V = IR$, and the R, C and frequency material from AD101. No calculus.

Course path

Work down this table in order. A Read row is one or more guide pages: concepts, figures and worked examples, with nothing to run. A Do row is one lab, where you run every command yourself. Each lab starts by listing the pages to read first.

#		What	Time
1	Read	Getting started · Resistors on a chip · Ohms per square · What a resistor costs in area	1.5 h
2	Do	Lab 01: A resistor you designed. Load the course, measure the sheet and end resistance of SKY130 poly, and size two resistors to within 1 % of their targets.	2.5 h
3	Read	Capacitors on a chip · What a picofarad costs · Parasitic capacitance · Inductors on a chip	1.5 h
4	Do	Lab 02: How big is a picofarad?. Fit a MIM capacitor's area and edge terms, size two capacitors, and measure the three inductors SKY130 ships.	2.5 h
5	Read	What to build instead of an inductor	30 min
6	Do	Lab 03: A time constant in silicon. Measure the time constant of your own resistor and capacitor in one circuit, then build a 20 ns RC in under 400 μm².	2 h
7	Read	Process corners · Matching and Pelgrom's law	1 h
8	Do	Lab 04: Two resistors that disagree. Run three process corners and a seeded Monte Carlo, then design a 0.45 V divider that is accurate, precise and under 150 μm².	2 h
9	Read	From schematic to cross-section	30 min

#		What	Time
10	Do	Capstone: Defend a floor plan. Read the layer stack, look at cross-sections in SiliWiz, and size a 1 MHz low-pass filter whose area you can defend.	1.5 h

The times are estimates, and they add up to the 15.5 hours above. There's no separate setup row, because setting up is the first part of Lab 01.

Keep these open while you work; they are for looking things up rather than reading through: The SKY130 passive catalogue · ngspice deck recipes

Stuck? Ask in the team Discord. Nobody expects you to work this out alone at 2 a.m. Getting help says what to put in your question.

What you'll do

1. Measure the sheet resistance of SKY130 high-sheet poly yourself. The model card (the PDK's SPICE description of the device) says 317.3885 Ω per square, but one drawn square simulates at 695.4646 Ω, more than twice that. You'll find where the extra ohms come from, then size a 10 kΩ resistor correctly on the first try (30.3315 µm long, landing at 9999.997 Ω), and two more of your own.
2. Work out what a picofarad costs in square micrometres, and why nobody puts a 1 µF capacitor on a chip.
3. Build an RC filter from the resistor and capacitor you designed and measure its time constant τ. Then measure its corner frequency, check it against $1/(2\pi\tau)$ to five figures, and compare its Bode plot with that of the same filter built from an ideal 10 kΩ and an ideal 1 pF: 15.8580 MHz for the filter you built against 15.9155 MHz for the ideal one, 0.36 % apart. Optionally, open the same circuit in XSchem and see a schematic turn into the device lines you have been editing by hand.
4. See the same resistor come out different at every process corner, and learn why analog designers build ratios rather than values.
5. Find out how you fabricate an inductor on a chip. Mostly you don't, so you'll also see what gets built instead.
6. Hit a filter spec using only devices the PDK actually ships, inside an area budget you have to defend.

The workbench

This course is pinned to the workbench image **`hpretl/iic-osic-tools:2026.08`**, which ships **ngspice-47** and **XSchem V3.4.8RC**. Tutorials online describe other versions, which have different flags, so when a command here disagrees with one you find online, use the one here: it's the one that runs on your machine. You'll check your versions in Lab 01, Part 1.

Each of Labs 01–04 has a **package**: a folder under `labs/` with its SPICE decks, a `Makefile` and a checker script. The packages run with `make` alone, with no environment setup, because every deck names its SKY130 model file by absolute path. You still do Lab 01, Part 1 once, to get the course files and check your tools. Apart from the SiliWiz parts, which run in a browser tab, every lab step runs in a terminal, and only the optional XSchem part of Lab 03 opens a window on the desktop. A fifth package, `passives-decks`, holds the decks whose output the guide pages quote, and some lab parts run it too. The capstone has no package, because all it needs is one command, a browser exercise and a page of arithmetic.

The first time you run each lab, its `make` ends in `FAIL`, and that's on purpose. Each package ships the design a first-year student would draw, usually sized straight off the model card, so that you read your own wrong number before you fix it. The message tells you which file to edit.

What you'll have at the end

You'll have a filter you designed from devices a real 130 nm process can make, simulated at every corner it will be manufactured at, with an area number you can defend. You'll also be in the habit of asking, for each part of an analog schematic, what shape it is and what it costs.

Next courses

- **AD103** — Nonlinear Circuits: the diode and the MOSFET, and the regions they operate in
- **AD104** — Layout: draw these devices yourself in Magic, DRC-clean and LVS-clean